**Anderson PUF Glitch Value Change Report**

**Introduction:**

This is a modification of the Anderson’s PUF Design by changing the glitch value from ‘1’ to ‘0’ from the reference of the paper “**On the re-design of an FPGA Based PUF**”.

**The Architecture of PUF Design:**

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VHDL Code:

-- Physically Unclonable Function (PUF) bit

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating

---- any Xilinx primitives in this code.

library UNISIM;

use UNISIM.VComponents.all;

entity PUF is

Port ( clk : in STD\_LOGIC;

out1 : out STD\_LOGIC;

shift\_in : in STD\_LOGIC

);

end PUF;

architecture Behavioral of PUF is

signal OUT\_INT : STD\_LOGIC;

signal CARRY\_OUT : STD\_LOGIC\_VECTOR(2 downto 0);

signal CARRY\_OUT2 : STD\_LOGIC\_VECTOR(2 downto 0);

signal dummy2 : STD\_LOGIC\_VECTOR(3 downto 0);

signal dummy3 : STD\_LOGIC\_VECTOR(3 downto 0);

signal OUT\_INT2 : STD\_LOGIC;

signal O1, O2 : STD\_LOGIC;

signal CARRY\_BW : STD\_LOGIC; -- the carry signal between 2 4-bit carry chains

signal shift\_in\_not : STD\_LOGIC := '0';

attribute rloc: string;

attribute rloc\_range : string;

-- These constraints ensure that the shift registers and carry chains

-- are located in the correct positions. (See ASP-DAC paper).

-- rloc: relative location constraints

-- Note that these constrain the sub-elements WITHIN a PUF bit.

-- The PUF bit itself is relocatable anywhere on the device.

attribute rloc of FDCPE\_inst: label is "X0Y1";

attribute rloc of CARRY4\_inst: label is "X0Y1";

attribute rloc of SRL16E\_inst: label is "X0Y1";

attribute rloc of CARRY4\_inst2: label is "X0Y0";

attribute rloc of SRL16E\_inst2: label is "X0Y0";

-- You can uncomment the lines below to constraint the PUF bit to a particular region on the Virtex-5 110 device

-- attribute rloc\_range of SRL16E\_inst: label is "X56Y0:X104Y53"; -- region 4

-- attribute rloc\_range of SRL16E\_inst: label is "X56Y54:X104Y106"; -- region 5

-- attribute rloc\_range of SRL16E\_inst: label is "X56Y107:X104Y159"; -- region 6

-- attribute rloc\_range of SRL16E\_inst: label is "X0Y0:X52Y53"; -- region 1

-- attribute rloc\_range of SRL16E\_inst: label is "X0Y54:X52Y106"; -- region 2

-- attribute rloc\_range of SRL16E\_inst: label is "X0Y107:X52Y159"; -- region 3

begin

shift\_in\_not <= not shift\_in;

SRL16E\_inst : SRL16E -- the "top" shift register instance

generic map (

INIT => X"5555")

port map (

Q => O1, -- SRL data output

A0 => '1', -- Select[0] input

A1 => '1', -- Select[1] input

A2 => '1', -- Select[2] input

A3 => '1', -- Select[3] input

CE => '1', -- Clock enable input

CLK => CLK, -- Clock input

D => shift\_in -- SRL data input

);

SRL16E\_inst2 : SRL16E -- the "bottom" shift register instance

generic map (

INIT => X"AAAA")

port map (

Q => O2, -- SRL data output

A0 => '1', -- Select[0] input

A1 => '1', -- Select[1] input

A2 => '1', -- Select[2] input

A3 => '1', -- Select[3] input

CE => '1', -- Clock enable input

CLK => CLK, -- Clock input

D => shift\_in\_not -- SRL data input

);

CARRY4\_inst : CARRY4 -- the "top" carry chain

port map (

CO(3) => OUT\_INT,

CO(2 downto 0) => CARRY\_OUT, -- 4-bit carry out

O => dummy2, -- 4-bit carry chain XOR data out

CI => CARRY\_BW, -- 1-bit carry cascade input

CYINIT => '0', -- 1-bit carry initialization

DI => "1111", -- 4-bit carry-MUX data in

S(3) => O1,

S(2) => '1',

S(1) => '1',

S(0) => '1'

);

CARRY4\_inst2 : CARRY4 -- the "bottom" carry chain

port map (

CO(3) => CARRY\_BW,

CO(2 downto 0) => CARRY\_OUT2, -- 4-bit carry out

O => dummy3, -- 4-bit carry chain XOR data out

CI => '0', -- 1-bit carry cascade input

CYINIT => '1', -- 1-bit carry initialization

DI => "1111", -- 4-bit carry-MUX data in

S(3) => '1',

S(2) => '1',

S(1) => O2,

S(0) => '1'

);

-- This FF detects the PULSE on the OUT\_INT signal

FDCPE\_inst : FDCPE

generic map (

INIT => '0') -- Initial value of register (?0? or ?1?)

port map (

Q => OUT\_INT2, -- Data output

C => CLK, -- Clock input

CE => '0', -- Clock enable input

CLR => '0', -- Asynchronous clear input

D => OUT\_INT2, -- Data input

PRE => OUT\_INT -- Asynchronous set input

);

FDCPE\_inst2 : FDCPE

generic map (

INIT => '0') -- Initial value of register (?0? or ?1?)

port map (

Q => OUT1, -- Data output

C => clk, -- Clock input

CE => '1', -- Clock enable input

CLR => '0', -- Asynchronous clear input

D => OUT\_INT2, -- Data input

PRE => '0' -- Asynchronous set input

);

end Behavioral;

**SCHEMATIC DIAGRAM:**

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**RESULTS:**

**FOR WITHOUT ANY CONSTRAINTS:**

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**FOR REGION 1:**

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**REGION 2:**

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